REMARKS

Claims 1, 5, and 7 have been amended. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made." No claims have been cancelled. Claim 8 has been added. Hence, claims 1-8 are pending.

Claim 7 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because "said first order" lacks proper antecedent basis. Claim 7 has been amended and is now believed to be in compliance with every paragraph of 35 U.S.C. § 112. Accordingly, the rejection to claim 7 under 35 U.S.C. § 112, second paragraph should be withdrawn.

Claims 1-4 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Cho (U.S. Patent No. 6,166,367). Claims 5-7 stand rejected under 35 U.S.C. § 103(a) as being unpatable over Cho in view of Adiletta (U.S. Patent No. 6,295,546). These rejections are respectfully traversed.

The present invention is directed to an image sensor system having a plurality of analog-to-digital converters (hereinafter "A/D converter(s)) each associated with a plurality of logical units. Each logical unit is comprised of a group of pixels. In one exemplary embodiment, the logical units are the columns of the pixel array. Specification, p. 28. However, logical units in alternate embodiment may instead be rows, or any other structure comprising multiple pixels. Specification, p. 31. Each A/D converter additionally is includes a plurality of storage locations. Each storage location is used to store the digital value converted from an analog signal of a pixel in a logical unit associated with that A/D converter.

The association between a single A/D converter and multiple logical units is often made in order to reduce the amount of require circuitry. For example, A/D converters are often shared between adjacent columns. In many instances, it is desirable to read the converted digital value in the same order as its placement. For example, it may be

desirable to read digital values of each adjacent column of a row. However, the A/D conversion process requires a finite amount of time and triggering shared A/D converters in the same order as the desired read order can result is slow performance due to the requirement to wait the finite amount of time between each conversion.

In the present invention, each A/D converter is associated with a plurality of logical units and further includes a corresponding plurality of storage locations. Each storage location is capable of storing a single converted digital value. Thus, if the A/D converter produces an 8-bit digital value, each storage location would be capable of storing 8-bits of data. See, e.g., specification, p. 29.

The storage locations are used to permit the A/D converts to be read in a desired read order which may be different from a conversion order. For example, if each A/D converter were associated with two adjacent columns, each A/D converter can be controlled to first convert and store a pixel signal from an odd column and then to convert and store a pixel signal from an even column. The converted value can then be read in column order by reading the storage locations in the desired order.

Accordingly, the independent claims include limitations directed to an A/D converter having N storage units (claim 1) or first and second storage elements (claim 5). Claims 1 and 5 further require each of the storage elements to store a converted digital value of an analog signal. For example, claim 1 recites: "a plurality of analog-to-digital converters, ... , each analog-to-digital converter including an ADC portion which receives an analog signal from one of said pixel sensors of a logical unit when said selector element is enabled, and converts said analog signal to a converted digital value, and N storage elements, each respectively associated with one of said plurality of analog to digital converter, and each for storing the converted digital value indicating the output signal."

Similarly, claim 5 recites: "receiving, in a plurality of A/D converter units, a respective plurality of signals from a respective plurality of first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a

respective plurality of first storage units; receiving, in said plurality of A/D converter units, a respective of signals from a respective plurality of second logical units, adjacent to said first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values in a respective plurality of second storage units."

Cho is directed to a programmable arithmetic circuit which may be used to form different circuit modules to perform different arithmetic operations which share common electronics elements so as to reduce the number of elements. Cho additionally discloses using the programmable arithmetic circuit to perform analog-to-digital conversion. Significantly, the analog-to-digital conversion process of Cho sequentially outputs different bits of the same analog-to-digital conversion. The portion of Cho relied upon by the Office Action (column 8, lines 18-24) describes a process where A/D conversion is performed by first calculating the most significant bit and then successively calculating each least significant bit until the least significant bit is converted. Cho therefore discloses the use of a single storage entry for an A/D converter. The circuitry disclosed by Cho is therefore not suitable for use in a system which shares an A/D converter between multiple logical unit and which permits converted digital values to be read out-of-order relative to the conversion order, since Cho does not include sufficient storage in its A/D converter to support out-of-order read out. Cho clearly does not teach or suggest the use of an A/D converter which includes multiple storage entries which store converted digital values, as required by the amended independent claims.

Adiletta is directed to a method for performing data scattering and retrieval such that certain calculations which normally require the use of a double ported memory can be performed using a single ported memory. Adieletta further discloses a method for performing discrete cosine transformation without requiring the use of a transpose matrix buffer. The Office Action cites a portion of Adieletta directed to big/little endian data format conversion for a teaching of reading information from an analog-to-digital converter in a different order in which the information was converted. However, Adieletta, like Cho, fails to teach or suggest the above recited limitations of the independent claims. Further,

neither Adieletta nor Cho are directed to imaging systems which share A/D converter between multiple logical unit and permit converted digital values to be read out-of-order relative to conversion order. It is respectfully submitted that there would be no motivation to combine the teachings of Cho and Adieletta. Further, even if the teachings of Cho and Adieletta were combined, it would not result in the claimed invention due to the lack of available storage to support out-of-order reading.

Claims 1 and 5 are therefore believed to be allowable over the prior art of record. Claims 2-4 and 8 (which depend from claim 1) and claims 6-7 (which depend from claim 5) are also believed to be allowable for these reasons and because the combination recited in the claims are not taught or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Please amend claims 1, 5, and 7 as follows:

1. An active pixel sensor device, comprising:

a sensor array of pixels, arranged in logical units, wherein each pixel comprises a photosensor element, an in-pixel buffer element, and an in-pixel selector element; and

[a pixel sensor array of photosensor elements, arranged in logical units, each photosensor element defining a pixel with a CMOS photosensor element, an in-pixel buffer element and an in-pixel selector element, said photosensor element arranged in an array; and]

a plurality of analog-to-digital converters, formed on the same substrate as said pixel sensor array, and each associated with N [at least two] logical units of the pixel sensor array, each analog-to-digital converter including an ADC portion which receives an analog signal from one of said pixel sensors of a logical unit when said selector element is enabled, and converts said analog signal to a converted digital value, and N [at least two unit] storage elements, each respectively associated with one of said plurality of analog to digital converter, and each for storing the converted digital value [one unit of digital information] indicating the output signal;[.]

wherein N is at least two.

5. A method of operating a pixel sensor array, comprising:

obtaining a pixel sensor array of photosensitive elements, each having a photosensitive element in a pixel, a buffer in said pixel associated with said photosensitive element, and a selector transistor in said pixel which is enabled to allow a signal from said pixel to pass, and disabled to block the signal from passing;

connecting a plurality of said outputs of said selector transistors to one another, to form a

plurality of logical units, each logical unit formed by a plurality of said output transistors which are connected to one another;

receiving, in a plurality of A/D converter units, a respective plurality of signals [image information] from a respective plurality of first logical units, [A/D converter units] and A/D converting said respective plurality of signals into a respective plurality of converted digital values [information] and [logically] storing said respective plurality of converted digital values information in a respective plurality of first storage units;

receiving, [information] in said plurality of A/D converter units, a respective of signals from a respective plurality of second logical units, adjacent to said first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and [logically] storing said [additional] respective plurality of converted digital values [information;] in a respective plurality of second storage units; and

reading out said information from said A/D conversion unit in a different order than an order in which the information was converted.

7. A method as in claim 5, wherein said units are linear units which are one of rows and columns, [said] and said different order include a first different order which skips lines between conversions, and a second different order which is a complete order.